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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/559,208	12/06/2005	Jose De Jesus Pineda De Gyvez	NL 030685	2758

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EXAMINER	
WHITMORE, STACY	
ART UNIT	PAPER NUMBER
2825	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/559,208	PINEDA DE GYVEZ ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments with respect to claims 2-10, and 12-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 2, 4-7, 9-10, and 12-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoberman (US Patent Application Publication 2004/0268278).

3. As for the claims, Hoberman discloses the invention as claimed, including:

16. (New) An integrated circuit, comprising:
a plurality of computation islands operating at one or more utility values, at least one utility value of a first computation island of the plurality of computation islands being different from a corresponding at least one utility value of a second computation island of the plurality of computation islands [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052]; and

a global monitor configured to monitor at least one working parameter related to a working condition of the integrated circuit [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

wherein each of the first and second computation islands comprises a local controller for independently tuning the corresponding at least one utility value based on the monitored at least one working parameter, the local controller communicating with a global controller to obtain a pre-set level of performance of the integrated circuit [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

17. (New) A method for real-time tuning of at least one utility value of an integrated circuit, comprising a plurality of computation islands operating at one or more utility values, each of the computation islands comprising a local controller for independently tuning the at least one utility value for the computation island, the method comprising:

monitoring at least one working parameter related to a working condition of the integrated circuit [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

independently tuning the at least one utility value for at least one computation island of the plurality of computation islands using the corresponding local controller, based on the monitored at least one working parameter [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052]; and

controlling each local controller of each computation island using a global controller to obtain a pre-set level of performance of the integrated circuit [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

18. (New) An integrated circuit, comprising:

a first computation island having a first value of a utility value, the first computation island comprising a first local controller and a first actuator [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

a second computation island having a second value of the utility value, the second computation island comprising a second local controller and a second actuator, the second computation island being isolated from the first computation island [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

an interface island for interfacing the first and second computation islands [fig. 1-2, element 265, 4; paragraphs 0013-0015, 0032-0047, 0052];
a global monitor configured to monitor a working parameter related to a working condition of the integrated circuit [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052]; and
a global controller configured to determine a range of the utility value for each of the first computation island and the second computation island based on the monitored working parameter [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052],
wherein each of the first and second local controllers obtains a pre-set level of performance of the integrated circuit from the global controller and independently tunes the utility value within the range of the utility value based on the monitored at least one working parameter [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052; especially paragraph 0047];
2. (Currently amended) The integrated circuit according to claim 16, wherein the one or more utility values comprise one or more of supply power (Vdd), transistor threshold voltage (Vt) or clock frequency (ck) [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];
4. (Currently amended) The integrated circuit according to claim 16, wherein the at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, logic noise margin values, threshold voltage value, or clock frequency value [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];
5. (Currently amended) The integrated circuit according to claim 16, wherein the pre-set level of performance relates to any least one of power consumption or speed of the integrated circuit [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];
6. (Currently amended) The integrated circuit according to claim 16, wherein each computation island is located in an isolated third well of a triple-well CMOS technology.
7. (Currently amended) The integrated circuit according to claim 16, furthermore further comprising- at least one interface island for interfacing among the plurality of computation islands [];

9. (Currently amended) The integrated circuit according to claim 16, wherein each of the first and second a computation islands further comprises an actuator for tuning the at least one utility value in a monitored utility value-regulating closed-loop system [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

10. (Currently amended) The integrated circuit according to claim 16, wherein each of the first and second a computation islands further comprises a local monitoring means for monitoring local working parameters of the computation island [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

12. (Currently amended) The method according to claim 17, wherein the at least one utility value comprises one or more of supply power (Vdd), transistor threshold voltage (Vt) or clock frequency (ck) [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

13. (Currently amended) The method according to claim 17, wherein the at least one working parameter comprises at least one of circuit activity, circuit delay, power supply noise, logic noise margin values, threshold voltage value, or clock frequency value [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

14. (Currently amended) The method according to claim 17, wherein the pre-set level of performance relates to at least one of power consumption or speed of the integrated circuit [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

15. (Currently amended) The method according to claim 17, wherein the integrated circuit is designed based on utility values different from nominal values [fig. 1-2, 4; paragraphs 0013-0015, 0032-0047, 0052];

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoberman (US Patent Application Publication 2004/0268278) in view of Chandrakasan (US Patent Application Publication (2004/0183588).

5. As for the claims, Hoberman discloses the invention substantially as claimed, including the integrated circuit as rejected above in claims 2, 7 and 16.

Hoberman does not specifically disclose:
3. (Currently amended) The integrated circuit according to claim 2, wherein the transistor threshold voltage is determined by a bulk voltage of at least one transistor in a computational island [paragraphs 0045-0046, substrate bias voltage];
8. (Currently amended) The integrated circuit according to claim 7, wherein at least two interface islands are located in a common third well, or a substrate, of a triple-well CMOS technology [paragraphs 0016, 0022-0023, 0060];

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hoberman and Chandrakasan because Both Hoberman and Chandrakasan are directed to the monitoring and control of utility values, performance improvement of integrated circuits involving computation islands. Further, Hoberman discloses that power or computational islands may be of section, delineation, partition, or division of the integrated circuit [paragraph 0032]. It therefore would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Hoberman and Chandrakasan to encompass voltage islands of transistors, including islands in wells, or triple well CMOS technology and including bulk voltage of those islands in order to gain control of concentrated or smaller circuits areas or devices to increase the level of monitoring and control for improved performance and power management.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stacy A Whitmore/
Primary Examiner
Art Unit 2825

SAW
June 27, 2008